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RESEARCH ARTICLE

AN ULTRA-LOW-POWER AND ULTRA-LOW –VOLTAGE 5 GHz LOW NOISE AMPLIFIER DESIGN WITH PRECISE CALCULATION

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ABSTRACT

In this paper a low-noise amplifier (LNA) is designed at 5GHz with the intention of ultra-low-power consumption. First, a spiral inductor is discussed and its equivalent circuit is described. Second, the input impedance, output impedance, and gain of a common-source LNA is calculated precisely. In addition, forward body biasing technique is used to bias all transistors to bring down the power consumption of the LNA. Plus, the comparison between precise calculation performed in this paper and the approximation proposed in other papers is demonstrated by HSPICE and MATLAB. The main simulation of the proposed LNA is carried out by Advanced Design System (ADS) and TSMC 0.18 um CMOS process is used for all elements in the LNA. The circuit is evaluated in different voltage supplies from 0.1 volt to 0.5 volt. The LNA is simulated with both lumped-elements and real elements. With lumped-elements the results are 0.96dB, -19dB, -16dB, 17.9dB, and 140μW for noise figure (NF), input impedance matching (S11), output impedance matching (S22), power gain (S21), and power consumption respectively. Plus, with real elements the results are 1.4dB, -20dB, -19dB, 15.4dB, and 139μW for noise figure (NF), input impedance matching (S11), output impedance matching (S22), power gain (S21), and power consumption respectively.

KEYWORDS

Forward Body Biasing, Precise Calculation, Spiral Inductor, Ultra-Low-Power, Ultra-Low-Voltage.

1. INTRODUCTION

A Low Noise Amplifier (LNA) is a decisive block in every RF receiver. The criteria by which an LNA can be evaluated are Noise Figure (NF), power consumption or dissipation (Pdiss), input and output impedance matching, linearity, and gain. The aforementioned criteria might be inefficient provided that the LNA is unstable. Hence, the stability of the LNA should be guaranteed by adjusting scattering parameters or S-parameters. Plus, input impedance matching, output impedance matching, and gain can be outlined by scattering parameters. In addition, the linearity of the LNA has been scrutinized by the third order intercept point (IIP3). Furthermore, the performance of an LNA against noise is to be analyzed by NF. In fact, the lower the NF is, the more appropriate the LNA will be.

All the comments are more suitable in an LNA with lower power dissipation brought about the voltage supply and the width of transistors. The purposes have been achieved by different topologies consisting of cascade, cascode, and differential [1-6]. Considering the bandwidth during which an LNA operates, LNAs can be categorized in two divergent classes, called narrow-band or wideband [7-10]. Furthermore, the size of transistors has been scaled down from micrometer to nanometer, thus bringing down the size of the LNA. The lifetime of LNAs is predicated upon the power they has consumed. Indeed, the lifetime will be considerably prolonged if the power consumption declines. The factor can diminish appreciably via decreasing the voltage supply, the size of transistors, and the method by which a transistor is biased. Plus, the methods should not sacrifice other worthwhile criteria such as gain and impedance matching as far as possible. Furthermore, owing to the fact that the elements within the designed LNA is supposed to calculated by the formula extracted from input matching, output matching, and gain, it is of prime significance to calculate the formulas precisely in order to attenuate the errors stemming from the formulas. In this paper, a three stage cascaded LNA is designed for the purpose of precise calculation, ultra-low-power, and ultra-low-voltage at 5GHz in 0.18 μm technology. In fact, the power consumption is diminished via *forward body biasing* technique.

2. SPIRAL INDUCTOR

Spiral inductors have been used widely as on-chip inductors. Unlike the lumped inductors, spiral inductors should not be considered as single elements with two terminals. The model utilized in this paper is demonstrated in figure 1 [11].

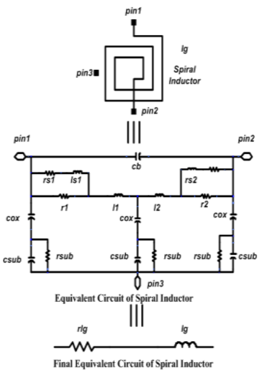

Figure 1: Spiral inductor and its equivalent circuits

All inductors are designed to function as a lumped inductor connected in series with a resistor, depicted in figure 1. In fact, spiral inductors can be designed according to their physical features, illustrated in figure 2. The inductance of a spiral inductor is given by [12]:

$$L=37.5\times\mu_0\times\left(\frac{n^2\times a^2}{22\times r-14\times a}\right) \quad (1)$$

In which:

$r = n \times (w+s)$

$\mu_0 = 4 \times \pi \times 10^{-7}$

n=number of turns
w=conductor width (m)
s= conductor spacing (m)
r= radius of the coil (m)
a= square spiral's mean radius (m)

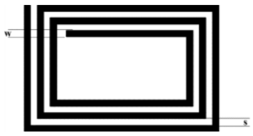

Figure 2: Spiral inductor

Therefore, the inductance can be designed by the number of turns and the radius of the device, which should fulfil the conditions in (2) to comply the restrictions existing in 0.18 μm technology.

$$\begin{cases} 30\mu m \le r \le 125\mu m \\ 1.5 \le n \le 5.5 \end{cases} \quad (2)$$

The number of turns and radius of the inductor are decisive factors by which the resistor in series with the final inductor can be defined. For instance, a 1nH inductor at 5GHz can be implemented by different number of turns and the radius of the device, producing different resistors, demonstrated in table 1. The inductor can be implemented by n=1.5 and n=2 with radius of 0.000082314009 meter and 0.000049037051 meter respectively. Plus, with different number of turns different resistors are created. Indeed, with bigger number of turns, bigger resistors are produced, influencing noise figure, linearity, biasing, and power consumption of the LNA. In addition, the implementation of the inductor (1nH) is impossible with n=2.5 and rad=0.000024569209 meter because of not fulfilling the conditions in (2). It is applicable to the number of turns which are more than 2.5. As a matter of fact, with n=5.5, the -0.00013485079 meter is achieved for radius to implement a 1nH inductor, which is impossible.

Table 1: Implementation of 1nh spiral inductor at 5ghz

n	Rad(m)	Resistor	w	lay
1.5	0.000082314009	2.6672	30 μm	6
2	0.000049037051	3.0486	30 μm	6
2.5 to 5.5	0.000024569209 to -0.00013485079	impossible	30 μm	6

3. THE PROPOSED LNA

The proposed LNA is composed of three common-source (CS) LNAs, demonstrated in figure 3. Hence, the CS LNA should be scrutinized meticulously. The significant factors by which an LNA is to be designed are input impedance, biasing, widths of transistors, capacitors, inductors, and output impedance. Therefore, a CS LNA is designed precisely and separately, depicted in figure 4.

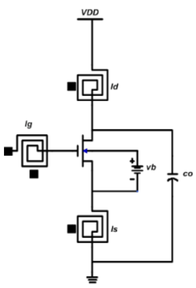

Figure 4: CS LNA with spiral inductors and forward body biasing

The common-source is biased with forward body biasing technique to bring down the voltage source, thus decreasing power consumption, shown in figure 4 [32]. As it is mentioned, all inductors, in this paper, are designed to operate as two terminal elements in series with resistors at the desired frequency, i.e. 5GHz. As a result, the CS LNS is considered with its equivalent circuit in the final design of spiral inductors, illustrated in figure 5.

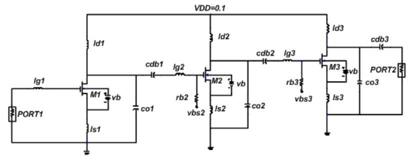

Figure 3: The proposed LNA

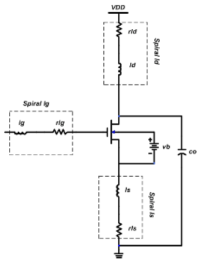

Figure 5: The CS LNA with equivalent circuit of spiral inductors

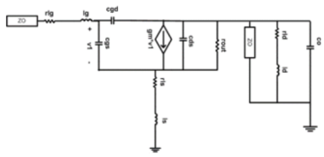

Figure 6: The AC equivalent circuit of figure 5

Next, in order to extract the input impedance (zin) of the circuit, the AC equivalent of the circuit should be taken into account, shown in figure 6. The input impedance of the circuit is given by [11-13]:

$$z_{in} \approx s \times (\lg + ls) + \frac{1}{s \times cgs} + \frac{gm \times ls}{cgs} \quad (3)$$

The formula implies that the elements exciting in the drain of the transistors are irrelevant to the input impedance. Plus, the resistors created by spiral inductors do not play any role in input impedance. In addition, the real part of zin does not vary via frequency. Therefore, the more precise calculation might be required to diminish the error brought about by the approximation of zin. The precise formula of zin is given by:

$$zin = \frac{NUMZIN}{DENZIN} \quad (4)$$

The details of (4) is represented in the Appendix.

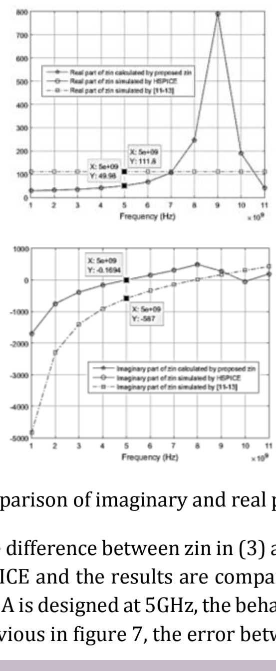

Figure 7: The comparison of imaginary and real part of proposed zin

In order to clarify the difference between zin in (3) and (4), the simulation is performed by HSPICE and the results are compared in figure 7. Owing to the fact that the LNA is designed at 5GHz, the behavior of the zin at 5GHz is focused. As it is obvious in figure 7, the error between the proposed zin and the zin simulated by HSIPCE is approximately zero. The zin in (3), on the other hand, has drastic error. For instance, the real part of zin with the proposed zin is 49.98 versus 111.8 coming from (3). Furthermore, the imaginary part of zin with the proposed zin is -0.1694 in comparison with -587 coming from (3). It is deduced from the comments that the elements calculated from (3) are not reliable enough and the simplicity or approximation might lead up to trial and error, which is not precise. The aforementioned comments are applicable to output impedance and gain of the LNA, given by:

$$ZOUT = \frac{NUMZOUT}{DENZOUT} \quad (5)$$

$$Gain = \frac{NUMGAIN}{DENGAIN} \quad (6)$$

The details of (5) and (6) are represented in the Appendix. In fact, the importance of precise calculation might be emphasized by knowing that all scattering parameters are dependent upon input impedance, output impedance, and gain, given by [14]:

$$\begin{cases} S11 = \frac{zin - zo}{zin + zo} \\ S22 = \frac{zout - zo}{zout + zo} \\ S21 = (1 + s11) \times (\frac{vout}{vin}) \\ S12 = (1 + s22) \times (\frac{vin}{vout}) \end{cases} \quad (7)$$

4. BIASING AND DESIGN

One of the main purpose of the design is to bring down power dissipation in the LNA. The forward body biasing technique might be beneficial with decreasing the supply voltage [32]. The *vdd* considered to fulfil the main goal is *0.1 volt.* Plus, the LNA has three stages which might appear to be the same. However, all transistors are biased in different regions. Indeed, M1 is biased in moderate inversion by which input impedance matching can be achieved. In addition, M2 is biased in moderate inversion with higher gate-source voltage with the intention of increasing gain. Ultimately, M3 is biased in strong inversion to have an appropriate gain and output impedance matching. Plus, the widths of transistors are equal to 100 μm.

5. RESULTAS AND TRADE-OFFS

The proposed LNA is simulated at 5 GHz by Advanced Design System (ADS) and 0.18μm CMOS Process is used for all transistors. The performance is evaluated in different situations, compared in table 2. First, the LNA is analyzed by lumped elements except transistors. Second, all elements, including inductors and capacitors, are substituted with their counterparts in 0.18 μm technology. Next, just lg1 from the first stage is replaced by a lumped inductor and results are extracted. Ultimately, all circumstances are scrutinized by increasing source voltage and the trade-offs are mentioned.

Table 1: Comparison Of The Performance Against Voltage Sources And Elements

Elements*	L	L	L	R	R	R	R
Vdd(volt)	0.1	0.3	0.5	0.1	0.1	0.3	0.5
NF(dB)	0.96	0.58	0.47	2.8	1.4	2.27	2.14
S11(dB)	-19	-18	-17	-20	-20	-16	-15
S22(dB)	-16	-15	-15	-19	-19	-15.9	-15
S12(dB)	-47	-48	-47	-48	-47	-49	-48
S21(dB)	17.9	22	23	14	15.4	18.8	20
Pdiss(μW)	140	515	946	139	139	510	937
μ	5.7	4.5	4	7.5	7.5	5	4.6

- R=REAL L=LUMPED (except transistors)

The results are demonstrated from figure 8 to figure 25. The trade-off between power consumption and noise figure in both lumped and real elements is observed. In fact, the higher the voltage supply is, the lower noise figure will be. In addition, the noise figure declines considerably by substituting lg1 with a lumped inductor. Indeed, the best input impedance matching and output impedance matching are achieved by the substitution of spiral lg1 for lumped lg1 with the minimum power consumption. The power gain of the LNA is in the best situation when vdd is increased to 0.5 volt. The progress, however, is gained by the expenditure of more power consumption, i.e. 937 or 946 micro watt.

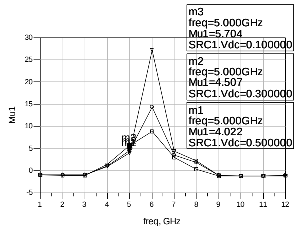

Figure 8: μ Stability with lumped-elements and vdd from 0.1 to 0.5

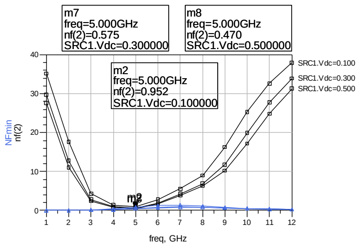

Figure 9: Noise Figure and Noise Figure minimum with lumped-elements and vdd from 0.1 to 0.5

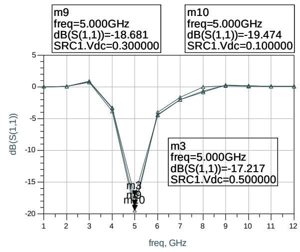

Figure 10: S11 with lumped-elements and vdd from 0.1 to 0.5

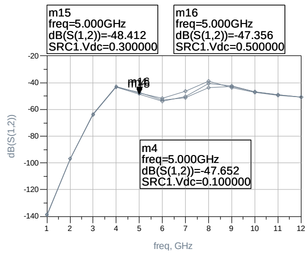

Figure 11: S12 with lumped-elements and vdd from 0.1 to 0.5

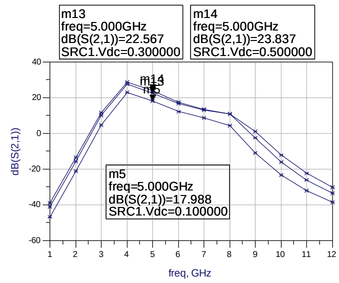

Figure 12: S21 with lumped-elements and vdd from 0.1 to 0.5

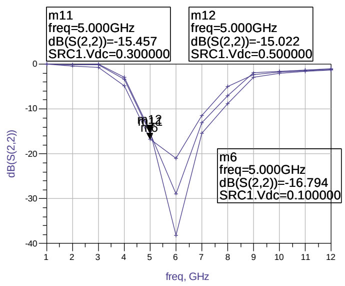

Figure 13: S22 with lumped-elements and vdd from 0.1 to 0.5

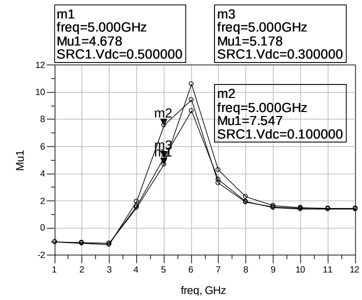

Figure 14: μ Stability with real elements and vdd from 0.1 to 0.5 and spiral lg1

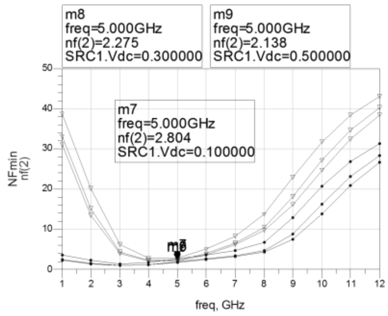

Figure 15: Noise Figure and Noise Figure minimum with real elements and vdd from 0.1 to 0.5 and spiral lg1

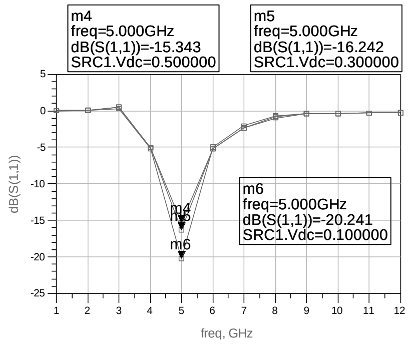

Figure 16: S11 with real elements and vdd from 0.1 to 0.5 and spiral lg1

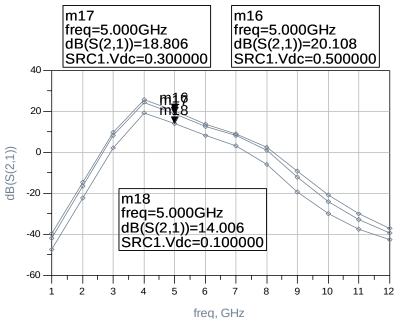

Figure 17: S21 with real elements and vdd from 0.1 to 0.5 and spiral lg1

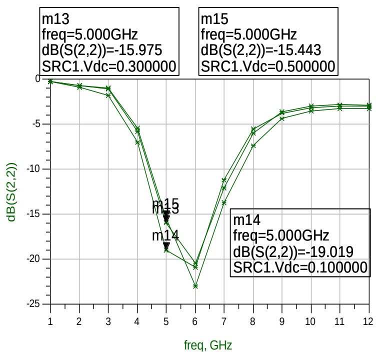

Figure 18: S22 with real elements and vdd from 0.1 to 0.5 and spiral lg1

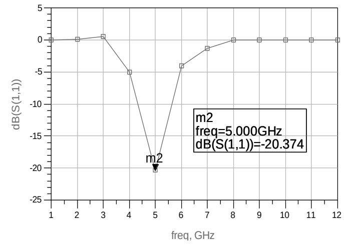

Figure 19: S11 with real elements and vdd=0.1 and lumped lg1

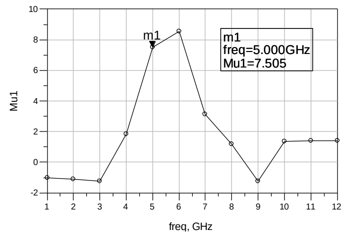

Figure 20: μ Stability with real elements and vdd=0.1 and lumped lg1

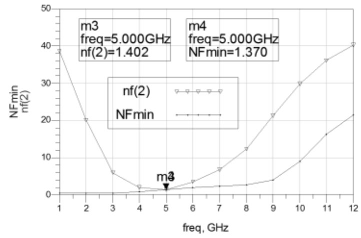

Figure 21: Noise Figure and Noise Figure minimum with real elements and vdd=0.1 and lumped lg1

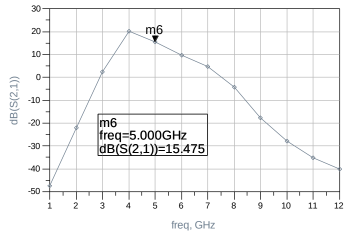

Figure 22: S21 with real elements and vdd=0.1 and lumped lg1

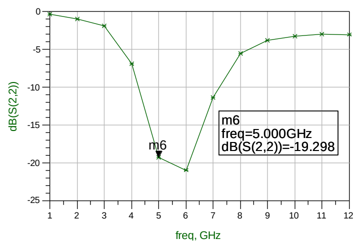

Figure 23: S22 with real elements and vdd=0.1 and lumped lg1

The operation of an LNA might be scrutinized more superior provided that all parameters participate to form criteria. The criteria can be created by three divergent figures of merit (FOM) given by [15], [17-18]:

$$FOM1 = \frac{20 \times \log|S21|}{P_{dc}} \quad (8)$$

$$FOM2 = \frac{|S21|}{|NF-1| \times P_{dc}} \quad (9)$$

$$FOM3 = \frac{Gain[abs] \times IIP3[mW] \times f_c[GHz]}{|NF-1|[abs] \times P_{dc}[mW]} \quad (10)$$

The results of the LNA is compared with other state-of-the-art in table 3. The best FOM belongs to the LNA with 0.1 volt and lumped elements. The

LNA has acceptable FOM when all elements are real except lg1. Even though all elements are real, the performance of the LNA when the supply voltage is 0.1 is suitable, especially when considering power consumption, i.e. 139 μW. All aforementioned criteria might be considered as useless if the LNA is not stable. Hence, mu (μ) stability test is used to evaluate the stability of the LNA, given by:

$$\begin{cases} \mu = \dfrac{1-|S11|^2-|S22|^2+|\Delta|^2}{2\times|S12|^2\times|S21|^2} \\ \Delta = S11\times S22 - S12\times S21 \end{cases} \quad (11)$$

In fact, the (μ) stability guarantees that the LNA is unconditionally stable provided that μ is larger than one. In addition, the larger μ is, the more stable the LNA will be. As it can be observed in table 2, the LNA is stable in all different voltage supplies. Moreover, the LNA is more stable when the voltage supply is 0.1 volt. Indeed, the LNA is more stable and power consumption is minimized by sacrificing the gain and noise figure.

The linearity of the LNA is assessed by IIP3, depicted in figure 24 and figure 25. The linearity is in the best situation with real elements versus the worst with lumped elements. Plus, the higher the supply voltage is, the less linear the LNA is.

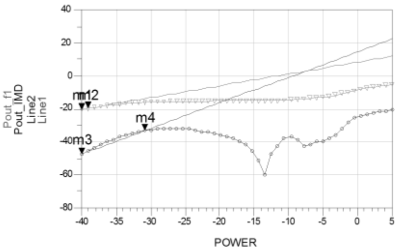

Figure 24: IIP3 with real elements and vdd=0.1

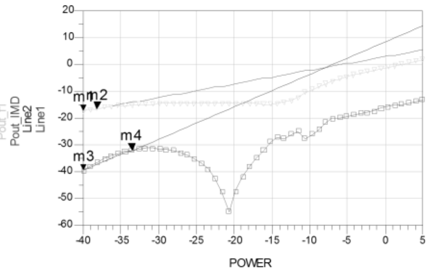

Figure 25: IIP3 with Lumped-elements and vdd=0.1

Table 2: Performance Summary And Comparison With Other State-Of-The-Art

	TECHNOLOGY	Frequency	Supply voltage	Power(diss)	S21	NF	S11	S22	IIP3	FOM1	FOM2	FOM3
unit	μm	GHz	V	mW	dB	dB	dB	dB	dBm	dB/mW	1/mW	-
This work + lumped	0.18	5	0.1	0.140	17.9	0.96	-19	-16	-9	127	2804	1765
This work + all real	0.18	5	0.1	0.139	14	2.8	-20	-19	-8	100	40	31
This work +all real except lg1	0.18	5	0.1	0.139	15.4	1.4	-20	-19	-9	110	211	133
This work+ lumped	0.18	5	0.5	0.946	23	0.47	-17	-15	-14	24	56	11
This work+ all real	0.18	5	0.5	0.937	20	2.14	-15	-15	-11	21	18	7
[19]	0.09	5.5	1.2	9.72	13	2.7	-11.7	-14	-3.25	1.34	0.53	1.39
[20]	0.09	5.5	0.6	2.1	11.2	3.6	-28	-14	-8.6	5.33	1.34	1.02
[21]	0.18	5	1.5	15	20	3.5	-20	-20	-9	1.33	0.54	0.34
[22]	0.18	5.8	1	22.2	13.2	2.5	-5.3	-10.3	-	0.59	0.26	-
	0.18	5.8	0.7	12.5	7	2.68	-7.1	-12.3	-	0.56	0.21	-
[23]	0.25	5.2	2	10	10	3	-30	-	0.3	1	0.32	1.77
	0.25	5.2	2	10	11	2.17	-45	-	0.3	1.1	0.55	3.05
[24]	0.25	5.25	3	12	14.4	2.8	-11.5	-12.3	-1.5	1.2	0.48	1.8
	0.25	5.25	3	24	16	2.5	-12.3	-11.9	-1.5	0.67	0.34	1.26
[25]	0.25	5.8	2	10	8	4.8	-23.5	-10.3	10	0.8	0.12	6.84
[26]	0.18	5.7	1.8	3.96	11.47	3.4	-14	-17	-	2.89	0.79	-
[27]	0.18	5.7	1	3.2	16.4	3.5	-11	-15	-	5.12	1.67	-
[28]	0.13	5.1	0.4	1.03	10.3	5.3	-17.7	-11.4	-	10.02	1.33	-
[29]	0.09	5.5	1.2	9.72	12.3	2.7	-10.3	-19	-3	1.27	0.49	0.68
[30]	0.09	5.5	0.6	1	9.2	3.6	-10	-14	-7.25	9.01	2.23	2.3
	0.09	5.5	0.8	5.4	14.4	2.9	-13.4	-10.7	-6.2	2.67	1.02	1.35
[31]	0.18	5	0.6	0.9	9.2	4.5	-12	-21	-16	10.22	1.76	0.23
[32]	0.18	5.2	0.6	1.08	10	3.37	-13.4	-10.6	-8.6	9.26	2.5	1.78
	0.18	5	0.6	1.68	14.1	3.65	-12.7	-14	-17.1	8.39	2.29	0.23
[33]	0.18	5.2	1.8	12.4	16.5	1.1	<-20	-13	-11.5	1.33	1.87	7.61
[34]	0.18	5.8	1.8	3.42	9.4	2.5	-13.3	-14.8	-7.6	2.75	1.11	1.16
[35]	0.18	5.4	1.8	2.7	21	2.8	<-10	-	-23	7.78	4.59	0.125
[36]	0.09	2.6-10.2	1.2	7.2	12.5	3-7	<-9	-	-	1.74	0.47	-
[37]	0.13	5.65	1.2	6.4	14.9	4.8	-32.4	-	-4.2	2.33	0.43	0.99
[38]	0.18	5	1.5	12	11	0.95	-33	-13	5	0.92	1.21	187
[15]	0.18	5.8	0.6	0.798	11.21	3.22	-19.1	-14.67	-9	14.04	4.14	3
	0.18	5.8	0.6	0.834	13.92	3.32	-12.74	-13.38	-11.5	16.69	5.19	2.1

6. CONCLUSION

This paper revolves around designing an LNA with the main focus on precise calculation and ultra-low-power consumption. The precise formulas are calculated to minimize the error coming from the calculation of input impedance, output impedance, and the gain. Indeed, forward body biasing technique contributes to diminishing the voltage supply, thus declining the power consumption. Different types of trade-offs are observed between power consumption, gain, noise figure, and linearity. Although the technology has been scaled down from micrometer to nanometer and this paper is in 0.18 μm, the calculations extracted in this paper are irrelevant to technology and applicable to other technologies. In addition, the LNA is not implemented and it is just designed and simulated. Nonetheless, it has been declared in other state-of-the-art that the simulation results are close to real results. Therefore, it might be deduced that if the LNA is implemented, the results might be close enough to the simulation results.

REFERENCES

[1] Fakharzadeh, M., Nezhad-Ahmadi, M.R., Biglarbegian, B., Ahmadi-Shokouh, J., Safavi-Naeini, S. 2010. CMOS phased array transceiver technology for 60GHz wireless applications. IEEE Transactions on Antennas and Propagation, 58, 1093–1104.

[2] Bozzola, S., Guermandi, D., Vecchi, F., Repossi, M., Pozzoni, M., Mazzanti, A., Svelto, F. 2009. A sliding IF receiver for mm-wave WLANs in 65 nm CMOS. IEEE CICC'09, 669–672.

[3] Parsa, A., Razavi, B. 2008. A 60 GHz CMOS receiver using a 30 GHz LO. ISSCC'08, 190–606.

[4] Yu, Y.K., Baltus, P.G.M., de Graauw, E., van der Heijden, E., Vaucher, C.S., van Roermund, A.H.M. 2010. A 60GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems. IEEE Journal of Solid-State Circuits, 45, 1697–1709.

[5] Fritsche, D., Tretter, G., Carta, C., Ellinger, F. 2015. Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS. IEEE Transactions on Microwave Theory and Techniques, 63, 1910–1922.

[6] Arbabian, A., Niknejad, A.M. 2009. Design of a CMOS tapered cascaded multistage distributed amplifier. IEEE Transactions on Microwave Theory and Techniques, 57, 938–947.

[7] Guo, B., Chen, J., Li, L., Jin, H., Yang, G. 2017. A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations. IEEE Journal of Solid-State Circuits, 52, 1331–1344.

[8] Pan, Z., Qin, C., Ye, Z., Wang, Y. 2017. A low power inductor less wideband LNA with Gm enhancement and noise cancellation. IEEE Microwave and Wireless Components Letters, 27, 58–60.

[9] Kuo, M.C., Kuo, C.N., Chueh, T.C. 2009. Wideband LNA compatible for differential and singleended inputs. IEEE Microwave and Wireless Components Letters, 19, 482–484.

[10] Kim, S.J., Lee, D., Lee, K.Y., Lee, S.G. 2017. A 2.4-GHz super-regenerative transceiver with selectivity-improving dual Q-enhancement architecture and 102-μW all-digital FLL. IEEE Transactions on Microwave Theory and Techniques, 65, 3287–3298.

[11] Yue, C.P., Ryu, C., Lau, J., Lee, T.H., Wong, S.S. 1996. A physical model for planar spiral inductors on silicon, in Proc. IEEE Int. Electron Devices Meeting, San Francisco, CA.

[12] Wheeler, H.A. 1928. Simple inductance formulas for radio coils. Proc. IRE, 16 (10), pp. 1398–1400.

[13] Cimino, M., Lapuyade, H., Deval, Y. 2008. Design of a 0.9 V 2.45 GHz self-testable and reliability-enhanced CMOS LNA. IEEE Journal of Solid-State Circuits, 43 (5), Pp. 1187-1194.

[14] Chen, K.H., Lu, J.H., Chen, B.J., Liu, S.L. 2007. An ultra-wide-band 0.4-10 GHz LNA in 0.18 μm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 54 (3), 217-221.

[15] Lai, M.T., Tsao, H.W. 2013. Ultra-low-power cascaded CMOS LNA with positive feedback and bias optimization. IEEE Transactions on Microwave Theory and Techniques, 61, 1934–1945.

[16] Gonzalez, G. 1997. Microwave Transistor Amplifiers: Analysis and Design, 2nd ed. Upper Saddle River. Englewood Cliffs, NJ, USA: Prentice-Hall.

[17] Linten, D., Thijs, S., Natarajan, M.I., Wambacq, P., Jeamsaksiri, W., Ramos, J., Mercha, A., Jenei, S., Donnay, S., Decoutere, S. 2005. A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS. IEEE J. Solid-State Circuits, 40 (7), Pp. 1434–1442.

[18] Brederlow, R., Weber, W., Sauerer, J., Donnay, S., Wambacq, P., Vertregt, M. 2001. A mixed signal design roadmap. IEEE Design Test Comput., 18 (6), Pp. 34–46.

[19] Jeamsaksiri, W., Mercha, A., Ramos, J., Linten, D., Thijs, S., Jenei, S., Detcheverry, C., Wambacq, P., Velghe, R., Decoutere, S. 2004. Integration of a 90 nm RF CMOS technology (200 GHz fmax—150 GHz fT NMOS) demonstrated on a 5 GHz LNA, in IEEE Symp. VLSI Technology Dig. Tech. Papers, pp. 100–101.

[20] Linten, D., Aspemyr, L., Jeamsaksiri, W., Ramos, J., Mercha, A., Jenei, S., Thijs, S., Garcia, R., Jacobsson, H., Wambacq, P., Donnay, S., Decoutere, S. 2004. Low-power 5 GHz LNA and VCO in 90 nm RF CMOS, in IEEE Symp. VLSI Circuits Dig. Tech. Papers, pp. 372–375.

[21] Leroux, P., Steyaert, M. 2004. A 5 GHz CMOS low-noise amplifier with inductive ESD protection exceeding 3 kV HBM. Proc Eur. Solid- State Circuits Conf., Sep., pp. 295–298.

[22] Tsang, T.K.K., El-Gamal, M. 2002. Gain and frequency controllable sub-1 V 5.8 GHz CMOS LNA. Proc. ISCAS, 4, pp. 795–798.

[23] Chiu, H.W., Lu, S.S. 2002. A 2.17 dB NF, 5 GHz band monolithic CMOS LNA with 10 mW DC power consumption. IEEE Symp. VLSI Circuits Dig. Tech. Papers, pp. 226–229.

[24] Westerwick, E.H. 2001. A 5 GHz band low noise amplifier with a 2.5 dB noise figure. Proc. IEEE Int. Symp. VLSI Technology, Systems, and Application, Apr. pp. 224–227.

[25] Mukherjee, D., Bhattacharjee, J., Chakaraborty, S., Laskar, J. 2002. A 5–6 GHz fully integrated CMOS LNA for a dual-band WLAN receiver. Proc. IEEE RAWCON, pp. 213–215.

[26] Asgaran, S., Deen, M.J., Chen, C.H. 2006. A 4-mW monolithic CMOS LNA at 5.7 GHZ with the gate resistance used for input matching, IEEE Microw. Wireless Compon. Lett., 16 (4), pp. 188–190.

[27] Wang, Y.S., Lu, L.H. 2005. 5.7 GHZ low-power variable-gain LNA in 0.18 m CMOS. Electron. Lett., 41, pp. 66–68.

[28] Wu, D.K., Huang, R., Wong, W., Wang, Y. 2007. A 0.4-V low noise amplifier using forward body bias technology for 5 GHZ application. IEEE Microw. Wireless Compon. Lett., 17 (7), Pp. 543–545.

[29] Linten, D., Thijs, S., Natarajan, M.I., Wambacq, P., Jeamsaksiri, W., Ramos, J., Mercha, A., Jenei, S., Donnay, S., Decoutere, S. 2005. A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS. IEEE J. Solid-State Circuits, 40 (7), Pp. 1434–1442.

[30] Linten, D., Aspemyr, L., Jeamsaksiri, W., Ramos, J., Mercha, A., Jenei, S., Thijs, S., Garcia, R., Jacobsson, H., Wambacq, P., Donnay, S., Decoutere, S. 2004. Low-power 5 GHZ LNA and vco in 90 nm RF CMOS. Proc. IEEE VLSI Circuits Symp, pp. 372–375.

[31] Hsieh, H.H., Lu, L.H. 2007. Design of ultra-low-voltage RF front ends with complementary current-reused architectures. IEEE Trans. Microw. Theory Techn., 55 (7), pp. 1445–1458.

[32] Hsieh, H.H., Wang, J.H., Lu, L.H. 2008. Gain-enhancement techniques for CMOS folded cascode LNAs at low-voltage operations. IEEE Trans. Microw. Theory Techn., 56 (8), pp. 1807–1816.

[33] Han, K., Gil, J., Song, S.S., Han, J., Shin, H., Kim, C.K., Lee, K. 2005. Complete high-frequency thermal noise modelling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier. IEEE J. Solid-State Circuits, 40 (3), pp. 726–735.

[34] Li, X., Shekhar, S., Allstot, D.J. 2005. A boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18 m CMOS. IEEE J. Solid-State Circuits, 40 (12), pp. 2609–2619.

[35] Walling, J.S., Shekhar, S., Allstot, D.J. 2007. A boosted current reuse LNA in 0.18 m CMOS. Proc. IEEE Radio Freq. Integr. Circuits Symp, pp. 613–616.

[36] Sapone, G., Palmisano, G. 2011. A 3–10 GHz low-power CMOS low noise amplifier for ultra-wideband communication. IEEE Trans. Microw. Theory Techn., 59 (3), pp. 678–686.

[37] Yu, X., Neihart, N.M. 2013. Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multi tap transformer. IEEE Trans. Microw. Theory Techn., 61 (3), pp. 1236–1246.

[38] A. Madan, M. J. McPartlin, C. Masse, W. Vaillancourt, and J. D. Cressler, A 5 GHZ 0.95 dB NF highly linear cascode floating-body LNA in 180 nm soi CMOS technology, IEEE Microw. Wireless Compon. Lett., vol. 22, no. 4, pp. 200–202.

APPENDIX

$$zin=\frac{NUMZIN}{DENZIN} \quad (A.1)$$

NUMZIN=(cgs×cgd×co×ld×lg×ls×rout×zo+cgs×cds×co×ld×lg×ls×rout×zo+cgd×cds×co×ld×lg×ls×rout×zo)×s^6+(cgs×cgd×ld×lg×ls×rout+cgs×cds×ld×lg×ls×rout+cgd×cds×ld×lg×ls×rout+cgs×co×ld×lg×ls×zo+cgd×co×ld×lg×ls×zo+cgd×co×gm×ld×lg×ls×rout×zo+cgs×cgd×co×ld×lg×rls×rout×zo+cgs×cds×co×ld×lg×rls×rout×zo+cgd×cds×co×ld×lg×rls×rout×zo+cgs×cgd×co×ld×ls×rlg×rout×zo+cgs×cds×co×ld×ls×rlg×rout×zo+cgd×cds×co×ld×ls×rlg×rout×zo+cgs×cgd×co×lg×ls×rld×rout×zo+cgs×cds×co×lg×ls×rld×rout×zo+cgd×cds×co×lg×ls×rld×rout×zo)×s^5+(cgs×ld×lg×ls+cgd×ld×lg×ls+cgd×gm×ld×lg×ls×rout+cgs×cgd×ld×lg×rls×rout+cgs×cds×ld×lg×rls×rout+cgd×cds×ld×lg×rls×rout+cgs×cgd×ld×ls×rlg×rout+cgs×cds×ld×ls×rlg×rout+cgd×cds×ld×ls×rlg×rout+cgs×cgd×lg×ls×rld×rout+cgs×cds×lg×ls×rld×rout+cgd×cds×lg×ls×rld×rout+cgs×cgd×ld×lg×rout×zo+cgs×cds×ld×lg×rout×zo+cgd×cds×ld×lg×rout×zo+cgs×cgd×ld×ls×rout×zo+cgs×cds×ld×ls×rout×zo+cgd×cds×ld×ls×rout×zo+cgs×cgd×lg×ls×rout×zo+cgs×cds×lg×ls×rout×zo+cgd×cds×lg×ls×rout×zo+cgs×co×ld×lg×rls×zo+cgd×co×ld×lg×rls×zo+cgs×co×ld×lg×rout×zo+cgd×co×ld×lg×rout×zo+cgs×co×ld×ls×rlg×zo+cgd×co×ld×ls×rlg×zo+cgs×co×lg×ls×rld×zo+cgd×co×lg×ls×rld×zo+cgs×co×ld×ls×rout×zo+cds×co×ld×ls×rout×zo+cgd×co×gm×ld×lg×rls×rout×zo+cgd×co×gm×ld×ls×rlg×rout×zo+cgd×co×gm×lg×ls×rld×rout×zo+cgs×cgd×co×ld×rlg×rls×rout×zo+cgs×cds×co×ld×rlg×rls×rout×zo+cgd×cds×co×ld×rlg×rls×rout×zo+cgs×cgd×co×lg×rld×rls×rout×zo+cgs×cds×co×lg×rld×rls×rout×zo+cgd×cds×co×lg×rld×rls×rout×zo+cgs×cgd×co×ls×rld×rlg×rout×zo+cgs×cds×co×ls×rld×rlg×rout×zo+cgd×cds×co×ls×rld×rlg×rout×zo)×s^4+(cgs×ld×lg×rls+cgd×ld×lg×rls+cgs×ld×lg×rout+cgd×ld×lg×rout+cgs×ld×ls×rlg+cgd×ld×ls×rlg+cgs×lg×ls×rld+cgd×lg×ls×rld+cgs×ld×ls×rout+cds×ld×ls×rout+cgs×ld×lg×zo+cgd×ld×lg×zo+cgs×ld×ls×zo+cgd×ld×ls×zo+cgs×lg×ls×zo+cgd×lg×ls×zo+co×ld×ls×zo+cgd×gm×ld×lg×rls×rout+cgd×gm×ld×ls×rlg×rout+cgd×gm×lg×ls×rld×rout+cgs×cgd×ld×rlg×rls×rout+cgs×cds×ld×rlg×rls×rout+cgd×cds×ld×rlg×rls×rout+cgs×cgd×lg×rld×rls×rout+cgs×cds×lg×rld×rls×rout+cgd×cds×lg×rld×rls×rout+cgs×cgd×ls×rld×rlg×rout+cgs×cds×ls×rld×rlg×rout+cgd×cds×ls×rld×rlg×rout+cgd×gm×ld×lg×rout×zo+cgd×gm×ld×ls×rout×zo+cgd×gm×lg×ls×rout×zo+co×gm×ld×ls×rout×zo+cgs×cgd×ld×rlg×rout×zo+cgs×cds×ld×rlg×rout×zo+cgd×cds×ld×rlg×rout×zo+cgs×cgd×ld×rls×rout×zo+cgs×cds×ld×rls×rout×zo+cgd×cds×ld×rls×rout×zo+cgs×cgd×lg×rld×rout×zo+cgs×cds×lg×rld×rout×zo+cgd×cds×lg×rld×rout×zo+cgs×cgd×lg×rls×rout×zo+cgs×cds×lg×rls×rout×zo+cgd×cds×lg×rls×rout×zo+cgs×cgd×ls×rld×rout×zo+cgs×cds×ls×rld×rout×zo+cgd×cds×ls×rld×rout×zo+cgs×cgd×ls×rlg×rout×zo+cgs×cds×ls×rlg×rout×zo+cgd×cds×ls×rlg×rout×zo+cgs×co×ld×rlg×rls×zo+cgd×co×ld×rlg×rls×zo+cgs×co×lg×rld×rls×zo+cgd×co×lg×rld×rls×zo+cgs×co×ld×rlg×rout×zo+cgd×co×ld×rlg×rout×zo+cgs×co×ld×rls×rout×zo+cds×co×ld×rls×rout×zo+cgs×co×lg×rld×rout×zo+cgd×co×lg×rld×rout×zo+cgs×co×ls×rld×rlg×zo+cgd×co×ls×rld×rlg×zo+cgs×co×ls×rld×rout×zo+cds×co×ls×rld×rout×zo+cgd×co×gm×ld×rlg×rls×rout×zo+cgd×co×gm×lg×rld×rls×rout×zo+cgd×co×gm×ls×rld×rlg×rout×zo+cgs×cgd×co×rld×rlg×rls×rout×zo+cgs×cds×co×rld×rlg×rls×rout×zo+cgd×cds×co×rld×rlg×rls×rout×zo)×s^3+(ld×ls+gm×ld×ls×rout+cgs×ld×rlg×rls+cgd×ld×rlg×rls+cgs×lg×rld×rls+cgd×lg×rld×rls+cgs×ld×rlg×rout+cgd×ld×rlg×rout+cgs×ld×rls×rout+cds×ld×rls×rout+cgs×lg×rld×rout+cgd×lg×rld×rout+cgs×ls×rld×rlg+cgd×ls×rld×rlg+cgs×ls×rld×rout+cds×ls×rld×rout+cgs×ld×rlg×zo+cgd×ld×rlg×zo+cgs×ld×rls×zo+cgd×ld×rls×zo+cgs×lg×rld×zo+cgd×lg×rld×zo+cgs×lg×rls×zo+cgd×lg×rls×zo+cgd×ld×rout×zo+cds×ld×rout×zo+cgs×lg×rout×zo+cgd×lg×rout×zo+cgs×ls×rld×zo+cgd×ls×rld×zo+cgs×ls×rlg×zo+cgd×ls×rlg×zo+cgs×ls×rout×zo+cds×ls×rout×zo+co×ld×rls×zo+co×ld×rout×zo+co×ls×rld×zo+cgd×gm×ld×rlg×rls×rout+cgd×gm×lg×rld×rls×rout+cgd×gm×ls×rld×rlg×rout+cgs×cgd×rld×rlg×rls×rout+cgs×cds×rld×rlg×rls×rout+cgd×cds×rld×rlg×rls×rout+cgd×gm×ld×rlg×rout×zo+cgd×gm×ld×rls×rout×zo+cg×gm×lg×rld×rout×zo+cgd×gm×lg×rls×rout×zo+cgd×gm×ls×rld×rout×zo+cgd×gm×ls×rlg×rout×zo+co×gm×ld×rls×rout×zo+co×gm×ls×rld×rout×zo+cgs×cgd×rld×rlg×rout×zo+cgs×cds×rld×rlg×rout×zo+cgd×cds×rld×rlg×rout×zo+cgs×cgd×rld×rls×rout×zo+cgs×cds×rld×rls×rout×zo+cgd×cds×rld×rls×rout×zo+cgs×cgd×rlg×rls×rout×zo+cgs×cds×rlg×rls×rout×zo+cgd×cds×rlg×rls×rout×zo+cgs×co×rld×rlg×rls×zo+cgd×co×rld×rlg×rls×zo+cgs×co×rld×rlg×rout×zo+cgd×co×rld×rlg×rout×zo+cgs×co×rld×rls×rout×zo+cds×co×rld×rls×rout×zo+cgd×co×gm×rld×rlg×rls×rout×zo)×s^2+(ld×rls+ld×rout+ls×rld+ld×zo+ls×zo+gm×ld×rls×rout+gm×ls×rld×rout+cgs×rld×rlg×rls+cgd×rld×rlg×rls+cgs×rld×rlg×rout+cgd×rld×rlg×rout+cgs×rld×rls×rout+cds×rld×rls×rout+gm×ls×rout×zo+cgs×rld×rlg×zo+cgd×rld×rlg×zo+cgs×rld×rls×zo+cgd×rld×rls×zo+cgs×rlg×rls×zo+cgd×rlg×rls×zo+cgd×rld×rout×zo+cds×rld×rout×zo+cgs×rlg×rout×zo+cgd×rlg×rout×zo+cgs×rls×rout×zo+cds×rls×rout×zo+co×rld×rls×zo+co×rld×rout×zo+cgd×gm×rld×rlg×rls×rout+cgd×gm×rld×rlg×rout×zo+cgd×gm×rld×rls×rout×zo+cgd×gm×rlg×rls×rout×zo+co×gm×rld×rls×rout×zo)×s+rld×rls+rld×rout+rld×zo+rls× zo+rout×zo+gm×rld×rls×rout+gm×rls×rout×zo

DENZIN=(cgs×cgd×co×ld×ls×rout×zo+cgs×cds×co×ld×ls×rout×zo+cgd×cds×co×ld×ls×rout×zo)×s^5+(cgs×cgd×ld×ls×rout+cgs×cds×ld×ls×rout+cgd×cds×ld×ls×rout+cgs×co×ld×ls×zo+cgd×co×ld×ls×zo+cgd×co×gm×ld×ls×rout×zo+cgs×cgd×co×ld×rls×rout×zo+cgs×cds×co×ld×rls×rout×zo+cgd×cds×co×ld×rls×rout×zo+cgs×cgd×co×ls×rld×rout×zo+cgs×cds×co×ls×rld×rout×zo+cgd×cds×co×ls×rld×rout×zo)×s^4+(cgs×ld×ls+cgd×ld×ls+cgd×gm×ld×ls×rout+cgs×cgd×ld×rls×rout+cgs×cds×ld×rls×rout+cgd×cds×ld×rls×rout+cgs×cgd×ls×rld×rout+cgs×cds×ls×rld×rout+cgd×cds×ls×rld×rout+cgs×cgd×ld×rout×zo+cgs×cds×ld×rout×zo+cgd×cds×ld×rout×zo+cgs×cgd×ls×rout×zo+cgs×cds×ls×rout×zo+cgd×cds×ls×rout×zo+cgs×co×ld×rls×zo+cgd×co×ld×rls×zo+cgs×co×ld×rout×zo+cgd×co×ld×rout×zo+cgs×co×ls×rld×zo+cgd×co×ls×rld×zo+cgd×co×gm×ld×rls×rout×zo+cgd×co×gm×ls×rld×rout×zo+cgs×cgd×co×rld×rls×rout×zo+cgs×cds×co×rld×rls×rout×zo+cgd×cds×co×rld×rls×rout×zo)×s^3+(cgs×ld×rls+cgd×ld×rls+cgs×ld×rout+cgd×ld×rout+cgs×ls×rld+cgd×ls×rld+cgs×ld×zo+cgd×ld×zo+cgs×ls×zo+cgd×ls×zo+cgd×gm×ld×rls×rout+cgd×gm×ls×rld×rout+cgs×cgd×rld×rls×rout+cgs×cds×rld×rls×rout+cgd×cds×rld×rls×rout+cgd×gm×ld×rout×zo+cgd×gm×ls×rout×zo+cgs×cgd×rld×rout×zo+cgs×cds×rld×rout×zo+cgd×cds×rld×rout×zo+cgs×cgd×rls×rout×zo+cgs×cds×rls×rout×zo+cgd×cds×rls×rout×zo+cgs×co×rld×rls×zo+cgd×co×rld×rls×zo+cgs×co×rld×rout×zo+cgd×co×rld×rout×zo+cgd×co×gm×rld×rls×rout×zo)×s^2+(cgs×rld×rls+cgd×rld×rls+cgs×rld×rout+cgd×rld×rout+cgs×rld×zo+cgd×rld×zo+cgs×rls×zo+cgd×rls×zo+cgs×rout×zo+cgd×rout×zo+cgd×gm×rld×rls×rout+cgd×gm×rld×rout×zo+cgd×gm×rls×rout×zo)×s

$$ZOUT=\frac{NUMZOUT}{DENZOUT} \quad (A.2)$$

NUMZOUT=ld×(cgs×cgd×lg×ls×rout+cgs×cds×lg×ls×rout+cgd×cds×lg×ls×rout)×s^5+(ld×(cgs×lg×ls+cgd×lg×ls+cgd×gm×lg×ls×rout+cgs×cgd×lg×rls×rout+cgs×cds×lg×rls×rout+cgd×cds×lg×rls×rout+cgs×cgd×ls×rlg×rout+cgs×cds×ls×rlg×rout+cgd×cds×ls×rlg×rout+cgs×cgd×ls×rout×zo+cgs×cds×ls×rout×zo+cgd×cds×ls×rout×zo)+rld×(cgs×cgd×lg×ls×rout+cgs×cds×lg×ls×rout+cgd×cds×lg×ls×rout))×s^4+(ld×(cgs×lg×rls+cgd×lg×rls+cgs×lg×rout+cgd×lg×rout+cgs×ls×rlg+cgd×ls×rlg+cgs×ls×rout+cds×ls×rout+cgs×ls×zo+cgd×ls×zo+cgd×gm×lg×rls×rout+cgd×gm×ls×rlg×rout+cgs×cgd×rlg×rls×rout+cgs×cds×rlg×rls×rout+cgd×cds×rlg×rls×rout+cgd×gm×ls×rout×zo+cgs×cgd×rls×rout×zo+cgs×cds×rls×rout×zo+cgd×cds×rls×rout×zo)+rld×(cgs×lg×ls+cgd×lg×ls+cgd×gm×lg×ls×rout+cgs×cgd×lg×rls×rout+cgs×cds×lg×rls×rout+cgd×cds×lg×rls×rout+cgs×cgd×ls×rlg×rout+cgs×cds×ls×rlg×rout+cgd×cds×ls×rlg×rout+cgs×cgd×ls×rout×zo+cgs×cds×ls×rout×zo+cgd×cds×ls×rout×zo))×s^3+(rld×(cgs×lg×rls+cgd×lg×rls+cgs×lg×rout+cgd×lg×rout+cgs×ls×rlg+cgd×ls×rlg+cgs×ls×rout+cds×ls×rout+cgs×ls×zo+cgd×ls×zo+cgd×gm×lg×rls×rout+cgd×gm×ls×rlg×rout+cgs×cgd×rlg×rls×rout+cgs×cds×rlg×rls×rout+cgd×cds×rlg×rls×rout+cgd×gm×ls×rout×zo+cgs×cgd×rls×rout×zo+cgs×cds×rls×rout×zo+cgd×cds×rls×rout×zo)+ld×(ls+gm×ls×rout+cgs×rlg×rls+cgd×rlg×rls+cgs×rlg×rout+cgd×rlg×rout+cgs×rls×rout+cds×rls×rout+cgs×rls×zo+cgd×rls×zo+cgs×rout×zo+cgd×rout×zo+cgd×gm×rlg×rls×rout+cgd×gm×rls×rout×zo))×s^2+(ld×(rls+rout+gm×rls×rout)+rld×(ls+gm×ls×rout+cgs×rlg×rls+cgd×rlg×rls+cgs×rlg×rout+cgd×rlg×rout+cgs×rls×rout+cds×rls×rout+cgs×rls×zo+cgd×rls×zo+cgs×rout×zo+cgd×rout×zo+cgd×gm×rlg×rls×rout+cgd×gm×rls×rout×zo))×s+rld×(rls+rout+gm×rls×rout)

DENZOUT=(cgs×cgd×co×ld×lg×ls×rout+cgs×cds×co×ld×lg×ls×rout+cgd×cds×co×ld×lg×ls×rout)×s^6+(cgs×co×ld×lg×ls+cgd×co×ld×lg×ls+cgd×co×gm×ld×lg×ls×rout+cgs×cgd×co×ld×lg×rls×rout+cgs×cds×co×ld×lg×rls×rout+cgd×cds×co×ld×lg×rls×rout+cgs×cgd×co×ld×ls×rlg×rout+cgs×cds×co×ld×ls×rlg×rout+cgd×cds×co×ld×ls×rlg×rout+cgs×cgd×co×lg×ls×rld×rout+cgs×cds×co×lg×ls×rld×rout+cgd×cds×co×lg×ls×rld×rout+cgs×cgd×co×ld×ls×rout×zo+cgs×cds×co×ld×ls×rout×zo+cgd×cds×co×ld×ls×rout×zo)×s^5+(cgs×cgd×ld×lg×rout+cgs×cds×ld×lg×rout+cgd×cds×ld×lg×rout+cgs×cgd×ld×ls×rout+cgs×cds×ld×ls×rout+cgd×cds×ld×ls×rout+cgs×cgd×lg×ls×rout+cgs×cds×lg×ls×rout+cgd×cds×lg×ls×rout+cgs×co×ld×lg×rls+cgd×co×ld×lg×rls+cgs×co×ld×lg×rout+cgd×co×ld×lg×rout+cgs×co×ld×ls×rlg+cgd×co×ld×ls×rlg+cgs×co×lg×ls×rld+cgd×co×lg×ls×rld+cgs×co×ld×ls×rout+cds×co×ld×ls×rout+cgs×co×ld×ls×zo+cgd×co×ld×ls×zo+cgd×co×gm×ld×lg×rls×rout+cgd×co×gm×ld×ls×rlg×rout+cgd×co×gm×lg×ls×rld×rout+cgs×cgd×co×ld×rlg×rls×rout+cgs×cds×co×ld×rlg×rls×rout+cgd×cds×co×ld×rlg×rls×rout+cgs×cgd×co×lg×rld×rls×rout+cgs×cds×co×lg×rld×rls×rout+cgd×cds×co×lg×rld×rls×rout+cgs×cgd×co×ls×rld×rlg×rout+cgs×cds×co×ls×rld×rlg×rout+cgd×cds×co×ls×rld×rlg×rout+cgd×co×gm×ld×ls×rout×zo+cgs×cgd×co×ld×rls×rout×zo+cgs×cds×co×ld×rls×rout×zo+cgd×cds×co×ld×rls×rout×zo+cgs×cgd×co×ls×rld×rout×zo+cgs×cds×co×ls×rld×rout×zo+cgd×cds×co×ls×rld×rout×zo)×s^4+(cgs×ld×lg+cgd×ld×lg+cgs×ld×ls+cgd×ld×ls+cgs×lg×ls+cgd×lg×ls+co×ld×ls+cgd×gm×ld×lg×rout+cgd×gm×ld×ls×rout+cgd×gm×lg×ls×rout+co×gm×ld×ls×rout+cgs×cgd×ld×rlg×rout+cgs×cds×ld×rlg×rout+cgd×cds×ld×rlg×rout+cgs×cgd×ld×rls×rout+cgs×cds×ld×rls×rout+cgd×cds×ld×rls×rout+cgs×cgd×lg×rld×rout+cgs×cds×lg×rld×rout+cgd×cds×lg×rld×rout+cgs×cgd×lg×rls×rout+cgs×cds×lg×rls×rout+cgd×cds×lg×rls×rout+cgs×cgd×ls×rld×rout+cgs×cds×ls×rld×rout+c gd×cds×ls×rld×rout+cgs×cgd×ls×rlg×rout+cgs×cds×ls×rlg×rout+cgd×cds×ls×rlg×rout+cgs×co×ld×rlg×rls+cgd×co×ld×rlg×rls+cgs×co×lg×rld×rls+cgd×co×lg×rld×rls+cgs×co×ld×rlg×rout+cgd×co×ld×rlg×rout+cgs×co×ld×rls×rout+cds×co×ld×rls×rout+cgs×co×lg×rld×rout+cgd×co×lg×rld×rout+cgs×co×ls×rld×rlg+cgd×co×ls×rld×rlg+cgs×co×ls×rld×rout+cds×co×ls×rld×rout+cgs×cgd×ld×rout×zo+cgs×cds×ld×rout×zo+cgd×cds×ld×rout×zo+cgs×cgd×ls×rout×zo+cgs×cds×ls×rout×zo+cgd×cds×ls×rout×zo+cgs×co×ld×rls×zo+cgd×co×ld×rls×zo+cgs×co×ld×rout×zo+cgd×co×ld×rout×zo+cgs×co×ls×rld×zo+cgd×co×ls×rld×zo+cgd×co×gm×ld×rlg×rls×rout+cgd×co×gm×lg×rld×rls×rout+cgd×co×gm×ls×rld×rlg×rout+cgs×cgd×co×rld×rlg×rls×rout+cgs×cds×co×rld×rlg×rls×rout+cgd×cds×co×rld×rlg×rls×rout+cgd×co×gm×ld×rls×rout×zo+cgd×co×gm×ls×rld×rout×zo+cgs×cgd×co×rld×rls×rout×zo+cgs×cds×co×rld×rls×rout×zo+cgd×cds×co×rld×rls×rout×zo)×s^3+(cgs×ld×rlg+cgd×ld×rlg+cgs×ld×rls+cgd×ld×rls+cgs×lg×rld+cgd×lg×rld+cgs×lg×rls+cgd×lg×rls+cgd×ld×rout+cds×ld×rout+cgs×lg×rout+cgd×lg×rout+cgs×ls×rld+cgd×ls×rld+cgs×ls×rlg+cgd×ls×rlg+cgs×ls×rout+cds×ls×rout+co×ld×rls+co×ld×rout+co×ls×rld+cgs×ld×zo+cgd×ld×zo+cgs×ls×zo+cgd×ls×zo+cgd×gm×ld×rlg×rout+cgd×gm×ld×rls×rout+cgd×gm×lg×rld×rout+cgd×gm×lg×rls×rout+cgd×gm×ls×rld×rout+cgd×gm×ls×rlg×rout+co×gm×ld×rls×rout+co×gm×ls×rld×rout+cgs×cgd×rld×rlg×rout+cgs×cds×rld×rlg×rout+cgd×cds×rld×rlg×rout+cgs×cgd×rld×rls×rout+cgs×cds×rld×rls×rout+cgd×cds×rld×rls×rout+cgs×cgd×rlg×rls×rout+cgs×cds×rlg×rls×rout+cgd×cds×rlg×rls×rout+cgs×co×rld×rlg×rls+cgd×co×rld×rlg×rls+cgs×co×rld×rlg×rout+cgd×co×rld×rlg×rout+cgs×co×rld×rls×rout+cds×co×rld×rls×rout+cgd×gm×ld×rout×zo+cgd×gm×ls×rout×zo+cgs×cgd×rld×rout×zo+cgs×cds×rld×rout×zo+cgd×cds×rld×rout×zo+cgs×cgd×rls×rout×zo+cgs×cds×rls×rout×zo+cgd×cds×rls×rout×zo+cgs×co×rld×rls×zo+cgd×co×rld×rls×zo+cgs×co×rld×rout×zo+cgd×co×rld×rout×zo+cgd×co×gm×rld×rlg×rls×rout+cgd×co×gm×rld×rls×rout×zo)×s^2+(ld+ls+gm×ls×rout+cgs×rld×rlg+cgd×rld×rlg+cgs×rld×rls+cgd×rld×rls+cgs×rlg×rls+cgd×rlg×rls+cgd×rld×rout+cds×rld×rout+cgs×rlg×rout+cgd×rlg×rout+cgs×rls×rout+cds×rls×rout+co×rld×rls+co×rld×rout+cgs×rld×zo+cgd×rld×zo+cgs×rls×zo+cgd×rls×zo+cgs×rout×zo+cgd×rout×zo+cgd×gm×rld×rlg×rout+cgd×gm×rld×rls×rout+cgd×gm×rlg×rls×rout+co×gm×rld×rls×rout+cgd×gm×rld×rout×zo+cgd×gm×rls×rout×zo)×s+rld+rls+rout+gm×rls×rout

$$\text{Gain}=\frac{\text{NUMGAIN}}{\text{DENGAIN}} \qquad (A.3)$$

NUMGAIN=ld×zo×(cgs×cgd×ls×rout+cgs×cds×ls×rout+cgd×cds×ls×rout)×s^4+(ld×zo×(cgs×ls+cgd×ls+cgd×gm×ls×rout+cgs×cgd×rls×rout+cgs×cds×rls×rout+cgd×cds×rls×rout)+rld×zo×(cgs×cgd×ls×rout+cgs×cds×ls×rout+cgd×cds×ls×rout))×s^3+(rld×zo×(cgs×ls+cgd×ls+cgd×gm×ls×rout+cgs×cgd×rls×rout+cgs×cds×rls×rout+cgd×cds×rls×rout)+ld×zo×(cgs×rls+cgd×rls+cgd×rout+cgd×gm×rls×rout))×s^2+(rld×zo×(cgs×rls+cgd×rls+cgd×rout+cgd×gm×rls×rout)-gm×ld×rout×zo)×s-gm×rld×rout×zo

DENGAIN=(cgs×cgd×co×ld×lg×ls×rout×zo+cgs×cds×co×ld×lg×ls×rout×zo+cgd×cds×co×ld×lg×ls×rout×zo)×s^6+(cgs×cgd×ld×lg×ls×rout+cgs×cds×ld×lg×ls×rout+cgd×cds×ld×lg×ls×rout+cgs×co×ld×lg×ls×zo+cgd×co×ld×lg×ls×zo+cgs×cgd×co×ld×ls×rout×zo^2+cgs×cds×co×ld×ls×rout×zo^2+cgd×cds×co×ld×ls×rout×zo^2+cgd×co×gm×ld×lg×ls×rout×zo+cgs×cgd×co×ld×lg×rls×rout×zo+cgs×cds×co×ld×lg×rls×rout×zo+cgd×cds×co×ld×lg×rls×rout×zo+cgs×cgd×co×ld×ls×rlg×rout×zo+cgs×cds×co×ld×ls×rlg×rout×zo+cgd×cds×co×ld×ls×rlg×rout×zo+cgs×cgd×co×lg×ls×rld×rout×zo+cgs×cds×co×lg×ls×rld×rout×zo+cgd×cds×co×lg×ls×rld×rout×zo)×s^5+(cgs×ld×lg×ls+cgd×ld×lg×ls+cgs×co×ld×ls×zo^2+cgd×co×ld×ls×zo^2+cgd×gm×ld×lg×ls×rout+cgs×cgd×ld×lg×rls×rout+cgs×cds×ld×lg×rls×rout+cgd×cds×ld×lg×rls×rout+cgs×cgd×ld×ls×rlg×rout+cgs×cds×ld×ls×rlg×rout+cgd×cds×ld×ls×rlg×rout+cgs×cgd×lg×ls×rld×rout+cgs×cds×lg×ls×rld×rout+cgd×cds×lg×ls×rld×rout+cgs×cgd×ld×lg×rout×zo+cgs×cds×ld×lg×rout×zo+cgd×cds×ld×lg×rout×zo+2×cgs×cgd×ld×ls×rout×zo+2×cgs×cds×ld×ls×rout×zo+2×cgd×cds×ld×ls×rout×zo+cgs×cgd×lg×ls×rout×zo+cgs×cds×lg×ls×rout×zo+cgd×cds×lg×ls×rout×zo+cgs×co×ld×lg×rls×zo+cgd×co×ld×lg×rls×zo+cgs×co×ld×lg×rout×zo+cgd×co×ld×lg×rout×zo+cgs×co×ld×ls×rlg×zo+cgd×co×ld×ls×rlg×zo+cgs×co×lg×ls×rld×zo+cgd×co×lg×ls×rld×zo+cgs×co×ld×ls×rout×zo+cds×co×ld×ls×rout×zo+cgd×co×gm×ld×ls×rout×zo^2+cgs×cgd×co×ld×rls×rout×zo^2+cgs×cds×co×ld×rls×rout×zo^2+cgd×cds×co×ld×rls×rout×zo^2+cgs×cgd×co×ls×rld×rout×zo^2+cgs×cds×co×ls×rld×rout×zo^2+cgd×cds×co×ls×rld×rout×zo^2+cgd×co×gm×ld×lg×rls×rout×zo+cgd×co×gm×ld×ls×rlg×rout×zo+cgd×co×gm×lg×ls×rld×rout×zo+cgs×cgd×co×ld×rlg×rls×rout×zo+cgs×cds×co×ld×rlg×rls×rout×zo+cgd×cds×co×ld×rlg×rls×rout×zo+cgs×cgd×co×lg×rld×rls×rout×zo+cgs×cds×co×lg×rld×rls×rout×zo+cgd×cds×co×lg×rld×rls×rout×zo+cgs×cgd×co×ls×rld×rlg×rout×zo+cgs×cds×co×ls×rld×rlg×rout×zo+cgd×cds×co×ls×rld×rlg×rout×zo)×s^4+(cgs×ld×lg×rls+cgd×ld×lg×rls+cgs×ld×lg×rout+cgd×ld×lg×rout+cgs×ld×ls×rlg+cgd×ld×ls×rlg+cgs×lg×ls×rld+cgd×lg×ls×rld+cgs×ld×ls×rout+cds×ld×ls×rout+cgs×ld×lg×zo+cgd×ld×lg×zo+2×cgs×ld×ls×zo+2×cgd×ld×ls×zo+cgs×lg×ls×zo+cgd×lg×ls×zo+co×ld×ls×zo+cgs×cgd×ld×rout×zo^2+cgs×cds×ld×rout×zo^2+cgd×cds×ld×rout×zo^2+cgs×cgd×ls×rout×zo^2+cgs×cds×ls×rout×zo^2+cgd×cds×ls×rout×zo^2+cgs×co×ld×rls×zo^2+cgd×co×ld×rls×zo^2+cgs×co×ld×rout×zo^2+cgd×co×ld×rout×zo^2+cgs×co×ls×rld×zo^2+cgd×co×ls×rld×zo^2+cgd×gm×ld×lg×rls×rout+cgd×gm×ld×ls×rlg×rout+cgd×gm×lg×ls×rld×rout+cgs×cgd×ld×rlg×rls×rout+cgs×cds×ld×rlg×rls×rout+cgd×cds×ld×rlg×rls×rout+cgs×cgd×lg×rld×rls×rout+cgs×cds×lg×rld×rls×rout+cgd×cds×lg×rld×rls×rout+cgs×cgd×ls×rld×rlg×rout+cgs×cds×ls×rld×rlg×rout+cgd×cds×ls×rld×rlg×rout+cgd×gm×ld×lg×rout×zo+2×cgd×gm×ld×ls×rout×zo+cgd×gm×lg×ls×rout×zo+co×gm×ld×ls×rout×zo+cgs×cgd×ld×rlg×rout×zo+cgs×cds×ld×rlg×rout×zo+cgd×cds×ld×rlg×rout×zo+2×cgs×cgd×ld×rls×rout×zo+2×cgs×cds×ld×rls×rout×zo+2×cgd×cds×ld×rls×rout×zo+cgs×cgd×lg×rld×rout×zo+cgs×cds×lg×rld×rout×zo+cgd×cds×lg×rld×rout×zo+cgs×cgd×lg×rls×rout×zo+cgs×cds×lg×rls×rout×zo+cgd×cds×lg×rls×rout×zo+2×cgs×cgd×ls×rld×rout×zo+2×cgs×cds×ls×rld×rout×zo+2×cgd×cds×ls×rld×rout×zo+cgs×cgd×ls×rlg×rout×zo+cgs×cds×ls×rlg×rout×zo+cgd×cds×ls×rlg×rout×zo+cgs×co×ld×rlg×rls×zo+cgd×co×ld×rlg×rls×zo+cgs×co×lg×rld×rls×zo+cgd×co×lg×rld×rls×zo+cgs×co×ld×rlg×rout×zo+cgd×co×ld×rlg×rout×zo+cgs×co×ld×rls×rout×zo+cds×co×ld×rls×rout×zo+cgs×co×lg×rld×rout×zo+cgd×co×lg×rld×rout×zo+cgs×co×ls×rld×rlg×zo+cgd×co×ls×rld×rlg×zo+cgs×co×ls×rld×rout×zo+cds×co×ls×rld×rout×zo+cgd×co×gm×ld×rls×rout×zo^2+cgd×co×gm×ls×rld×rout×zo^2+cgs×cgd×co×rld×rls×rout×zo^2+cgs×cds×co×rld×rls×rout×zo^2+cgd×cds×co×rld×rls×rout×zo^2+cgd×co×gm×ld×rlg×rls×rout×zo+cgd×co×gm×lg×rld×rls×rout×zo+cgd×co×gm×ls×rld×rlg×rout×zo+cgs×cgd×co×rld×rlg×rls×rout×zo+cgs×cds×co×rld×rlg×rls×rout×zo+cgd×cds×co×rld×rlg×rls×rout×zo)×s^3+(ld×ls+cgs×ld×zo^2+cgd×ld×zo^2+cgs×ls×zo^2+cgd×ls×zo^2+gm×ld×ls×rout+cgs×ld×rlg×rls+cgd×ld×rlg×rls+cgs×lg×rld×rls+cgd×lg×rld×rls+cgs×ld×rlg×rout+cgd×ld×rlg×rout+cgs×ld×rls×rout+cds×ld×rls×rout+cgs×lg×rld×rout+cgd×lg×rld×rout+cgs×ls×rld×rlg+cgd×ls×rld×rlg+cgs×ls×rld×rout+cds×ls×rld×rout+cgs×ld×rlg×zo+cgd×ld×rlg×zo+2×cgs×ld×rls×zo+2×cgd×ld×rls×zo+cgs×lg×rld×zo+cgd×lg×rld×zo+cgs×lg×rls×zo+cgd×lg×rls×zo+cgs×ld×rout×zo+2×cgd×ld×rout×zo+cds×ld×rout×zo+cgs×lg×rout×zo+cgd×lg×rout×zo+2×cgs×ls×rld×zo+2×cgd×ls×rld×zo+cgs×ls×rlg×zo+cgd×ls×rlg×zo+cgs×ls×rout×zo+cds×ls×rout×zo+co×ld×rls×zo+co×ld×rout×zo+co×ls×rld×zo+cgd×gm×ld×rout×zo^2+cgd×gm×ls×rout×zo^2+cgs×cgd×rld×rout×zo^2+cgs×cds×rld×rout×zo^2+cgd×cds×rld×rout×zo^2+cgs×cgd×rls×rout×zo^2+cgs×cds×rls×rout×zo^2+cgd×cds×rls×rout×zo^2+cgs×co×rld×rls×zo^2+cgd×co×rld×rls×zo^2+cgs×co×rld×rout×zo^2+cgd×co×rld×rout×zo^2+cgd×gm×ld×rlg×rls×rout+cgd×gm×lg×rld×rls×rout+cgd×gm×ls×rld×rlg×rout+cgs×cgd×rld×rlg×rls×rout+cgs×cds×rld×rlg×rls×rout+cgd×cds×rld×rlg×rls×rout+cgd×gm×ld×rlg×rout×zo+2×cgd×gm×ld×rls×rout×zo+cgd×gm×lg×rld×rout×zo+cgd×gm×lg×rls×rout×zo+2×cgd×gm×ls×rld×rout×zo+cgd×gm×ls×rlg×rout×zo+co×gm×ld×rls×rout×zo+co×gm×ls×rld×rout×zo+cgs×cgd×rld×rlg×rout×zo+cgs×cds×rld×rlg×rout×zo+cgd×cds×rld×rlg×rout×zo+2×cgs×cgd×rld×rls×rout×zo+2×cgs×cds×rld×rls×rout×zo+2×cgd×cds×rld×rls×rout×zo+cgs×cgd×rlg×rls×rout×zo+cgs×cds×rlg×rls×rout×zo+cgd×cds×rlg×rls×rout×zo+cgs×co×rld×rlg×rls×zo+cgd×co×rld×rlg×rls×zo+cgs×co×rld×rlg×rout×zo+cgd×co×rld×rlg×rout×zo+cgs×co×rld×rls×rout×zo+cds×co×rld×rls×rout×zo+cgd×co×gm×rld×rls×rout×zo^2+cgd×co×gm×rld×rlg×rls×rout×zo)×s^2+(ld×rls+ld×rout+ls×rld+ld×zo+ls×zo+cgs×rld×zo^2+cgd×rld×zo^2+cgs×rls×zo^2+cgd×rls×zo^2+cgs×rout×zo^2+cgd×rout×zo^2+gm×ld×rls×rout+gm×ls×rld×rout+cgs×rld×rlg×rls+cgd×rld×rlg×rls+cgs×rld×rlg×rout+cgd×rld×rlg×rout+cgs×rld×rls×rout+cds×rld×rls×rout+gm×ls×rout×zo+cgs×rld×rlg×zo+cgd×rld×rlg×zo+2×cgs×rld×rls×zo+2×cgd×rld×rls×zo+cgs×rlg×rls×zo+cgd×rlg×rls×zo+cgs×rld×rout×zo+2×cgd×rld×rout×zo+cds×rld×rout×zo+cgs×rlg×rout×zo+cgd×rlg×rout×zo+cgs×rls×rout×zo+cds×rls×rout×zo+co×rld×rls×zo+co×rld×rout×zo+cgd×gm×rld×rout×zo^2+cgd×gm×rls×rout×zo^2+cgd×gm×rld×rlg×rls×rout+cgd×gm×rld×rlg×rout×zo+2×cgd×gm×rld×rls×rout×zo+cgd×gm×rlg×rls×rout×zo+co×gm×rld×rls×rout×zo)×s+rld×rls+rld×rout+rld×zo+rls×zo+rout×zo+gm×rld×rls×rout+gm×rls×rout×zo

In which:
rout: the output resistor of the transistor
zo: the impedance of input or output port
cgd: the capacitor seen through gate-to-drain of the transistor
cds: the capacitor seen through drain-to-source of the transistor
cgs: the capacitor seen through gate-to-source of the transistor
gm: transconductance of the transistor
rlg: the resistor created by spiral inductor lg
rls: the resistor created by spiral inductor ls
rld: the resistor created by spiral inductor ld

$s: 2\times\pi\times f\times\sqrt{-1}$

f: frequency